					ATTY. DOCKET NO.		APPLICATION NO			
	1	FORM F	PTO-1449		SP038.C5 (1397.0140005) To Be Assigned 10/815,742 FIRST NAMED INVENTOR					
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EXAMINER		LDOG	NI INACATE	U.S. PA	ATENT DOCUMENTS					
INITIAL			UMENT IBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE		
RIE	AA1	4,62	26,989	12/02/1986	Torii	_	_			
RIE	AB1		75,806	06/23/1987	Uchida	_	~			
RUE	AC1		2,049	01/26/1988	Lahti			_		
RIE	AD1		7,115	02/21/1989	Torng			_		
THE	AE1		23,201	04/18/1989	Simon et al.			_		
RIE	AF1	4,90	3,196	02/20/1990	Pomerene et al.	-		-		
RÆ	AG1	4,94	2,525	07/17/1990	Shintani et al.	_				
RIE	AH1	5,06	7,069	11/19/1991	Fite et al.	_	_ _			
RUE	Al1	5,07	2,364	12/10/1991	Jardine et al.	-		_		
RVE	AJ1	5,10	9,495	04/28/1992	Fite et al.	_	-	_		
RIE	AK1	5,12	5,083	06/23/1992	Fite et al.			_		
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EXAMINER INITIAL	-		UMENT IBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION		
	AL1		88/09035	11/1988	PGF WIPO		_	Yes No		
	AM1		5 166	11/1992	EPO EPO			Yes No		
RLE	AN1	H2-4	18732	02/19/1990	Japan			Yes No		
	· · ·		OTHER (I	ncluding Auth	or, Title, Date, Pertinent P	ages, et	(c.)			
RIE	AO	1	Acosta, R. D. o	et al., "An Instruction On Computers, IEEE	n Issuing Approach to Enhancing Perf , Vol. C-35, No. 9, pp. 815-828 (Septe	formance in ember 1986)	Multiple Functional Ui	nit Processors," IEEE		
RLE	AP	1	Agerwala, T. a 31, 1987).	Agerwala, T. and Cocke, J., "High Performance Reduced Instruction Set Processors," IBM Research Division, pp. 1-61 (March 31, 1987).						
RLE	AR	1	Butler, M. and Ann Arbor, M	Butler, M. and Patt, Y., "An Improved Area-Efficient Register Alias Table for Implementing HPS," University of Michigan, Ann Arbor, Michigan, 24 pages (January 1990).						
RLIZ	AS	1	Butler, M. et a Symposium on	Butler, M. et al., "Single Instruction Stream Parallelism Is Greater than Two," Proceedings of the 18th Annual International Symposium on Computer Architecture, ACM, pp. 276-286 (May 1991).						
" RUE"	ĂT.	1	Charlesworth, A.E., "An Approach to Scientific Array Processing: The Architectural Design of the AP-120B/FPS-164 Family," Computer, IEEE, Vol. 14, pp. 18-27 (September 1981).							
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EXAMINER: Initia and not considere	al if referenced. Include	ence co le copy	nsidered, whet of this form wit	her or not citation i h next communica	s in conformance with MPEP 609. tion to Applicant.	Draw line	through citation if no	t in conformance		

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INFORMATION DISCLOSURE STATEMENT

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	ATTY. DOCKET NO.	APPLICATION NO	D. 1
	SP038.C5 (1397.0140005)	To Be Assigned	10/8/5,742
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RUE A82 5,148,536 09/15/1992 Witek et al.	EXAMINER				DATE	NAME	CLASS	CLID CLASS	EU INIC DATE
Ref AB2 5,167,026 11/24/1992 Murray et al.		AA2						SUB-CLASS	FILING DATE
RUE AC2 5,179,673 01/12/1993 Steely, Jr. et al.		AB2	5,167	',026	11/24/1992	Murray et al.		_	
RUE AP2 5,197,132 03/23/1993 Steely, Jr. et al.		AC2	5,179	,673	01/12/1993	Steely, Jr. et al.			+
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AF2 5,222,240 06/22/1993 Pate	RUE	AE2	5,214	,763	03/25/1993	Blaner et al.			+
RE AG2 5,226,126 07/06/1993 McFarland et al.		AF2	5,222	,240	06/22/1993	Patel			†
AH2 5,230,068 07720/1993 Van Dyke et al. AI2 5,251,306 10/05/1993 Tran AI2 5,251,306 10/05/1993 Tran AI2 5,317,720 05/31/1994 Stamm et al. AI2 5,345,569 09/06/01994 Tran FOREIGN PATENT DOCUMENTS EXAMINER NITIAL DOCUMENT NUMBER DATE COUNTRY CLASS SUB-CLASS TRANSLATION NO N		AG2	5,226	,126	07/06/1993	McFarland et al.			+
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Foster, C.C. and Riseman, E.M., "Percolation of Code to Enhance Parallel Dispatching and Execution," <i>IEEE Transactions On Computers</i> , IEEE, pp. 1411-1415 (December 1971). REF. AS. 2. Gee, J. et al., "The Implementation of Prolog via VAX 8600 Microcode," <i>Proceedings of Micro 19</i> , IEEE, October 1986, pp. 68-74. AT 2 Gross, T.R. and Hennessy, J.L., "Optimizing Delayed Branches," <i>Proceedings of the 5th Annual Workshop on Microprogramming</i> , IEEE, pp. 114-120 (October 5-7, 1982). EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance.	RUE	AO	2	Colwell, R.P.	et al., "A VLIW Ard ral Support for Prog	chitecture for a Trace Schedulin gramming Languages and Opera	ng Compiler," Proceeding Systems, ACM, pp	ngs of the 2nd Inter 5. 180-192 (Octobe	rnational Conference τ 1987).
Computers, IEEE, pp. 1411-1415 (December 1971). Computers, IEEE, pp. 1411-1415 (December 1971). Computers, IEEE, pp. 1411-1415 (December 1971). Computer	RUE	AP	2	Dwyer, H, A-/	Multiple, Out-of-Ora	ler Instruction Issuing System fo	or Superscalar Processo	ors, UMI, pp. 1-249	9 (August 1991).
Gross, T.R. and Hennessy, J.L., "Optimizing Delayed Branches," Proceedings of the 5th Annual Workshop on Microprogramming, IEEE, pp. 114-120 (October 5-7, 1982). EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance.	RUE	AR	Foster, C.C. and Riseman, E.M., "Percolation of Code to Enhance Parallel Dispatching and Execution," <i>IEEE Transactions On Computers</i> , IEEE, pp. 1411-1415 (December 1971).						
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INITIAL		NUM		DATE	NAME	CLASS	SUB-CLASS	FILING DATE
RUE	AA3	5,355	5,457	10/11/1994	Shebanow et al.	-		
RUE	AB3	5,367	,660	11/22/1994	Gat et al.	_		-
RIE	AC3	5,390	,355	02/14/1995	Horst		_	_
RE	AD3	5,398	,330	03/14/1995	Johnson		_	
RUE	AE3	5,430	,888,	07/04/1995	Witek et al.	,	_	
RUE	AF3	5,442		08/15/1995	McFarland et al.		_	
RUE	AG3	5,487		01/23/1996	Popescu et al.			
RUE	AH3	5,560		09/24/1996	Nguyen et al.			-
RUE	AI3	5,561		10/01/1996	Popescu et al.	-	,	_
RUE	AJ3	5.568		10/22/1996	Sites et al.	_	_	
RIE	AK3	5,574	,927	11/12/1996	Scantlin			~
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RŒ	AO	3	Hennessy, J.L		Computer Architecture: A Quantity			ublishers, pp. xi-xv,
PUE	AP	3	Hwu, W-M. V Computers, II	V. and Patt, Y.N., "CEE, Vol. C-36, No.	Checkpoint Repair for High-Performa 12, pp. 1496-1514 (December 1987)	nce Out-of-Order	Execution Machine	s," IEEE Trans. On
RUE	AR	3	Hwu, W. and Patt, Y., "Design Choices for the HPSm Microprocessor Chip," Proceedings of the Twentieth Annual Hawaii International Conference on System Sciences, pp. 330-336 (1987).					
RUE	Hwu, W-M. W. and Chang, P.P., "Exploiting Parallel Microprocessor Microarchitectures with a Compiler Code Generator," Proceedings of the 15th Annual Symposium on Computer Architecture, IEEE, pp. 45-53 (June 1988).							
RCE	Hwu, W-M. et al., "An HPS Implementation of VAX: Initial Design and Analysis," Proceedings of the Nineteenth Annual Hawaii International Conference on System Sciences, pp. 282-291 (1986).							teenth Annual
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RUE	AA4	5,592	2,636	01/07/1997	Popescu et al.	_	_			
RUE	AB4	5,625	5,837	04/29/1997	Popescu et al.	_				
RUE	AC4	5,627	,983	05/06/1997	Popescu et al.			1_		
RUE	AD4	5,630	,149	05/13/1997	Bluhm					
RIE	AE4	5,651	,125	07/22/1997	Witt et al.					
RUE	AF4	5,708	3,841	01/13/1998 🖘	Popescu et al.					
RUE	AG4	5,768	,575	06/16/1998	McFarland et al.					
RUE	AH4	5,778	,210	07/07/1998	Henstrom et al.		_	1		
ROE	Al4	5,797	,025	08/18/1998	Popescu et al.	-	1.	 		
RUE	AJ4	5,826	,055	10/20/1998	Wang et al.	-	-	 		
RUE	AK4	5,832	2,205	11/03/1998	Kelly et al.			_		
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	AN4							Yes No		
			OTHER (Including Aut	hor, Title, Date, Pertinen	Pages, etc.)	<u> </u>	140		
RIE	AO	4	Hwu, W-M. a	nd Patt, Y.N., "HPS	m, a High Performance Restricted D , pp. 297-306 (June 2-5, 1986).			al Functionality,"		
RLE	AP	4	Hwu, W. and	Patt, Y., "HPSm2: A	A Refined Single-Chip Microengine,	" HICSS '88, IEEE	pp. 30–40 (1988).			
RUE	AR	4	IBM Journal o	BM Journal of Research and Development, IBM, Vol. 34, No. 1, pp. 1-70 (January 1990).						
RLE	AS	4	Johnson, M. S	ohnson, M. Superscalar Microprocessor Design, Prentice-Hall, pp. vii-xi and 87-125 (1991).						
RLE	AT	4	Johnson, W. M	A., Super-Scalar Pro	ocessor Design, (Dissertation), 134 p			· · · · · · · · · · · · · · · · · · ·		
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RUE	AA5	5,832,		11/03/1998	Popescu et al.	•			
RUE	AB5	6,131,	157	10/10/2000	Wang et al.		_	~.	
RUE	AC5	6,412,	064	06/25/2002	Wang et al.	-	<i></i>	/	
ROE	AD5	5,961,	629	10/05/1999	Nguyen et al.		_		
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RUE	AO	<u>5</u>	Jouppi, N.P. as Proceedings of	nd Wall, D.W., "Ava	ilable Instruction-Level Parallelism fo Il Conference on Architectural Suppor	r Superscalar a	nd Superpipelined h	Machines," I Operating Systems,	
RUE RUE RUE	AP	<u>5</u>	Keller, R.M., "Look-Ahead Processors," Computing Surveys, ACM, Vol. 7, No. 4, pp. 177-195 (December 1975).						
RLE	AR	<u>5</u>	Lightner, B.D. and Hill, G., "The Metaflow Lightning Chipset", Compcon Spring 91, IEEE, pp. 13-18 (February 25 - March 1, 1991).						
RIE	AS	<u>5</u>	Patt, Y.N. et al., "Critical Issues Regarding HPS, A High Performance Microarchitecture", Proceedings of 18th Annual Workshop on Microprogramming, IEEE, pp. 109-116 (December 3-6, 1985).						
RUE	AT	<u>5</u>	Hwu et al., "E COMPCON 8	Experiments with HI 86, IEEE, pp. 254-25	PS, a Restricted Data Flow Microard 8 (1986).	chitecture for I	ligh Performance	Computers,"	
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ATTY. DOCKET NO.	APPLICATION NO.
SP038.C5 (1397.01400)5) To Be Assigned 10\&15,742
FIRST NAMED INVENTOR	
WANG et al.	
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ATTY. DOCKET NO. SP038.C5 (1397.0140005)	APPLICATION NO. To Be Assigned 10/8/5/742
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INFORMATION DISCLOSURE STATEMENT

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ATTY. DOCKET NO. SP038.C5 (1397.0140005)	APPLICATION NO. To Be Assigned 10815,742
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	ATTY. DOCKET NO. SP038.C5 (1397.0140005)	APPLICATION NO. To Be Assigned	
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